IN THE CLAIMS

Following are the current claims. Applicant respectfully notes that the claims have NOT been amended in this Response, so any differences between the following claims and the actual current claims are unintentional and in the nature of a typographic error:

1. (Previously Presented) A tunable quadrature phase shifter, comprising:

an input means for inputting an input signal;

splitting means for splitting the input signal into two essentially orthogonal first and second signals;

adding means for adding said first and second signals;

subtracting means for subtracting said first and second signals;

a first output for outputting a first output signal based on the output signal from said adding means; and

a second output for outputting a second output signal based on the output signal from said subtracting means, wherein said splitting means is an all-pass.

2. (Previously Presented) The phase shifter of claim 1, further comprising a first output buffer means for buffering said first output signal, and a second output buffer means for buffering said second output signal.

3. (Previously Presented) The phase shifter of claim 1, further comprising a first transimpedance converter having its input connected to said input means.

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4. (Previously Presented) The phase shifter of claim 1, further comprising a first transimpedance converter having its output connected to said first output, and a second transimpedance converter having its output connected to said second output.

5. (Previously Presented) The phase shifter of claim 3, wherein the transimpedance converter is a transimpedance amplifier.

6. (Previously Presented) The phase shifter of claim 2, wherein said first and second output buffer means are first and second transimpedance converters, respectively.

7. (Previously Presented) The phase shifter of claim 1, the splitting means comprising at least a first transistor with its collector connected to its base and its emitter coupled to a predetermined potential, a second transistor with its base connected to the base of said first transistor and its emitter coupled to said predetermined fixed potential, and a capacitor coupled between the junction of the bases of said first and second transistor and said predetermined potential.

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8. (Previously Presented) The phase shifter of claim 1, the splitting means comprising:

a first input for inputting an input signal;

a second input for inputting an inverse input signal;

a first transistor with its collector connected to its base and its emitter coupled to a predetermined potential;

a second transistor with its base connected to the base of said first transistor and its emitter coupled to said predetermined potential;

a third transistor with its collector connected to its base and its emitter coupled to a predetermined potential;

a fourth transistor with its base connected to the base of said third transistor and its collector coupled to said predetermined potential; and

a capacitor coupled between a first junction of the bases of said first and second transistors and a second junction of the bases of said third and fourth transistors.

9. (Previously Presented) The phase shifter of claim 7, wherein said transistors are npn transistors.

10. (Previously Presented) The phase shifter of claim 7, wherein said predetermined potential is zero.

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11. (Previously Presented) A data and clock recovery unit comprising a phase detector which includes a phase shifter having

an input means for inputting an input signal;

splitting means for splitting the input signal into two essentially orthogonal first and second signals;

adding means for adding said first and second signals;

subtracting means for subtracting said first and second signals;

a first output for outputting a first output signal based on the output signal from said adding means; and

a second output for outputting a second output signal based on the output signal from said subtracting means, wherein said splitting means is an all-pass.

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